Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (previously presented): A method of processing a semiconductor wafer that reduces plasma-induced damage to the wafer, said method comprising creating a plasma in a reaction chamber and performing all of the following in the sequence indicated while maintaining said plasma in said a reaction chamber:

inserting the wafer into the reaction chamber;

processing the wafer in the plasma;

cooling the wafer by an amount sufficient to terminate processing the wafer; and

removing the wafer from the reaction chamber.

Claim 2 (previously presented): The method of Claim 1, wherein the wafer reaches a process temperature during processing and a removal temperature during removing, and wherein the removal temperature is at least between about 100°C and about 500°C below the process temperature.

Claim 3 (previously presented): The method of Claim 2, wherein the process temperature is greater than about 300°C and the removal temperature is less than about 300°C.

Claim 4 (previously presented): The method of Claim 2, wherein the removal temperature is between about 80°C and about 300°C.

Claim 5 (previously presented): The method of Claim 1, further comprising cooling the wafer to between about 15°C and 30°C before inserting the wafer into the reaction chamber.

Claim 6 (previously presented): The method of Claim 1, wherein processing the wafer comprises the deposition of silicon dioxide.

Claim 7 (previously presented): The method of Claim 6, wherein the wafer reaches a temperature between about 275°C and 325°C during processing.

SILICON VALLEY
'ATENT GROUP LLP
50 Mission College Blvd
Suite 360
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

Claim 8 (previously presented): The method of Claim 1, wherein processing the wafer comprises the deposition of fluorine doped silicon dioxide.

Claim 9 (previously presented): The method of Claim 8, wherein the wafer reaches a temperature between about 325°C and 375°C during processing.

Claim 10 (previously presented): The method of Claim 1, wherein processing the wafer comprises the deposition of silicon dioxide for shallow trench isolation.

Claim 11 (previously presented): The method of Claim 10, wherein the wafer reaches a temperature between about 400°C and 550°C during processing.

Claim 12 (previously presented): The method of Claim 1, wherein processing the wafer comprises the deposition of phosphorus-doped silicon dioxide.

Claim 13 (previously presented): The method of Claim 12, wherein the wafer reaches a temperature between about 400°C and 550°C during processing.

Claim 14 (previously presented): The method of Claim 1, wherein processing the wafer comprises the etching of photoresist.

Claim 15 (previously presented): The method of Claim 1, wherein cooling the wafer lasts between about 2 seconds and about 30 seconds.

Claim 16 (original): The method of Claim 1, wherein cooling the wafer to a removal temperature comprises blowing a gas over the wafer.

Claim 17 (canceled)

Claim 18 (original): The method of Claim 1, wherein the wafer comprises a gate dielectric layer.

Claim 19 (canceled)

Claim 20 (canceled)

Claim 21 (canceled)

Claim 22 (canceled)

Claim 23 (canceled)

SILICON VALLEY
'ATENT GROUP LLP

50 Mission College Blvd
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(408) 982-8200
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Claim 24 (canceled)

Claim 25 (previously presented): The method of Claim 1 wherein cooling the wafer comprises reducing the power supplied to the plasma.

Claim 26 (previously presented): The method of Claim 25 wherein reducing the power comprises reducing the source RF power supplied to the plasma.

Claim 27 (new): The method of Claim 1 wherein cooling the wafer comprises cooling a platen on which the wafer rests.

Claim 28 (new): The method of Claim 1, further comprising cooling the wafer before inserting the wafer into the reaction chamber.

SILICON VALLEY
'ATENT GROUP LLP

50 Mission College Blvd
Suite 360
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